

PTO/SB/08a(08/03)

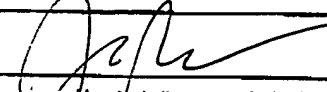
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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>			Application Number	09/932,330	
			Filing Date	August 17, 2001	
			First Named Inventor	Jon M. Huppentha et al.	
			Art Unit	2154	
			Examiner Name	Not Yet Assigned	
Sheet	1	of	1	Attorney Docket No.	SRC012

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No. ¹	Document No. No. - Kind Code ²	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Doc	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
JN		US-6,052,134	04/18/2000	Foster	Column 3, lines 12-25; column 5, lines 30 to column 8, line 12; column 6, lines 63 to column 7 line 10.
JN		US-4,972,457	11/20/1990	O'Sullivan	Column 4, lines 3-12, column 5, lines 50-55; column 7, lines 7-41.
JN		US-6,452,700 B1	08/17/2002	Mays, Jr.	Column 4, lines 20-42.
JN		US-5,889,959	03/30/1999	Whittaker et al.	Column 4, lines 42-49.
JN		US-6,581,157 B1	08/17/2003	Chiles et al.	Column 8, line 55 to column 9 line 8.
JN		US-6,480,014 B1	11/12/2002	Li et al.	Column 2, lines 47-56.
		US-			
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FOREIGN PATENT DOCUMENTS						
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This collection of information is required by 37 CFR 1.87 and 1.89. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) and application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

PTO/SB/08A (10/01)
(Substitute for form 1449A/PTO)

ATTY. DOCKET NO. SRC012
Client/Matter No. 80404.0015

APPLICATION NO.
09/932,330

INFORMATION DISCLOSURE
STATEMENT BY APPLICANT

FIRST NAMED INVENTOR

Jon M. Huppenthal, Thomas R. Seeman, Lee A. Burton

FILING DATE
August 17, 2001

ART UNIT
2154

(Use several sheets if necessary)

Sheet 1 of 1

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	Document No. No. - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Doc	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
JN		US-6,076,152	06/13/2000	Huppenthal et al.	
JN		US-6,052,773	04/18/2000	DeHon et al.	
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FOREIGN PATENT DOCUMENTS

Examiner Initials	Cite No.	Foreign Patent Doc cntry code - No. - Kind Code	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Doc	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear	TRANSLATION	
						YES	NO

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s) publisher, city and/or country where published
JN		YUN, HYUN-KYU AND SILVERMAN, H. F.; "A distributed memory MIMD multi-computer with reconfigurable custom computing capabilities", Brown University, 10-13 Dec. 1997, pp. 7-13.

EXAMINER SIGNATURE

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PTO/SB/08A (10/01) (Replaces Form 1449A/PTO) INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary) Sheet <u>1</u> of <u>1</u>		ATTY. DOCKET NO. SRC012 Client/Matter N . 80404.0015		APPLICATION NO. 09/932,330	
		FIRST NAMED INVENTOR Jon M. Huppenthal, Thomas R. Seeman, Le. A. Burton			
		FILING DATE August 17, 2001		ART UNIT 2154	

OCT 11 2002
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JN		US-5,903,771	05/11/1999	Sgro et al.	Figs 1 & 6, col. 3, lines 30-67, col 4, lines 1-51, col 7, lines 1-27.
JN		US-6,192,439	02/20/2001	Grunewald et al.	Fig 3, col 3, lines 53-67, col 4, lines 1-64.
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						YES	NO

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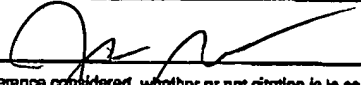
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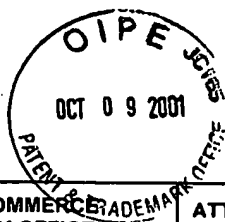
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Sheet 1 of 3

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(Modified) PATENT AND TRADEMARK OFFICE

ATTY. DOCKET NO. SRC0012

SERIAL NO. 09/932,330

INFORMATION DISCLOSURE
STATEMENT BY APPLICANT

APPLICANT: Jon M. HUPPENTHAL, et al.

(Use several sheets if necessary)

FILING DATE: August 17, 2001

GROUP 2154

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	PATENT NUMBER	ISSUE DATE	PATENTEE	CLASS	SUBCLAS S	FILING DATE IF APPROPRIATE
JN	5,230,057	07/20/93	Shido, et al.			
JN	5,892,962	04/06/99	Cloutier			

FOREIGN PATENT OR PUBLISHED FOREIGN PATENT APPLICATION

	DOCUMENT NUMBER	PUBLISH DATE	COUNTRY	CLASS	SUBCLAS S	TRANSLATION	
						YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

JN	AGARWAL, A., et al., "The Raw Compiler Project", pages 1-12, http://cag-www.lcs.mit.edu/raw , Proceedings of the Second SUIF Compiler Workshop, Augs. 21-23, 1997.
JN	ALBAHARNA, OSAMA, et al., "On the viability of FPGA-based integrated coprocessors", © 1996 IEEE, Publ. No. 0-8186-7548-9/96, Pages 206-215.
JN	AMERSON, RICK, et al., "Teramac—Configurable Custom Computing", © 1995 IEEE, Publ. No. 0-8186-7086-X/95, Pages 32-38.
JN	BARTHEL, DOMINIQUE August 25-26, 1997, "PVP a Parallel Video coProcessor", Hot Chips IX, Pages 203-210.
JN	BERTIN, PATRICE, et al., "Programmable active memories: a performance assessment", © 1993 Massachusetts Institute of Technology, Pages 88-102.
JN	BITTNER, RAY, et al., "Computing kernels implemented with a wormhole RTR CCM", © 1997 IEEE, Publ. No. 0-8186-8159-4/97, Pages 98-105.
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JN	CASSELMAN, STEVEN, "Virtual Computing and The Virtual Computer", © 1993 IEEE, Publ. No. 0-8186-3890-7/93, Pages 43-48.
JN	CHAN, PAK, et al., "Architectural tradeoffs in field-programmable-device-based computing systems", © 1993 IEEE, Publ. No. 0-8186-3890-7/93, Pages 152-161.
JN	CLARK, DAVID, et al., "Supporting FPGA microprocessors through retargetable software tools", © 1996 IEEE, Publ. No. 0-8186-7548-9/96, Pages 195-103.
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JW	CULBERTSON, W. BRUCE, et al., "Exploring architectures for volume visualization on the Teramac custom computer", © 1996 IEEE, Publ. No. 0-8186-7548-9/96, Pages 80-88.
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JN	GOKHALE, M., et al., "Processing in Memory: The Terasys Massively Parallel PIM Array" © April 1995, IEEE, Pages 23-31.
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JN	HOGEL, H., et al., "Enable++: A second generation FPGA processor", © 1995 IEEE, Publ. No. 0-8186-7086-X/95, Pages 45-53.
JN	KING, WILLIAM, et al., "Using MORRPH in an industrial machine vision system". © 1996 IEEE, Publ. No. 08186-7548-9/96, Pages 18-26.
JN	MANOHAR, SWAMINATHAN, et al., "A pragmatic approach to systolic design", © 1988 IEEE, Publ. No. CH2603-9/88/0000/0463, Pages 463-472.
JN	MAUDUIT, NICOLAS, et al., "Lneuro 1.0: a piece of hardware LEGO for building neural network systems," © 1992 IEEE, Publ. No. 1045-9227/92, Pages 414-422.
JN	MIRSKY, ETHAN A., "Coarse-Grain Reconfigurable Computing", Massachusetts Institute of Technology, June 1996.
JN	MIRSKY, ETHAN, et al., "MATRIX: A Reconfigurable Computing Architecture with Configurable Instruction Distribution and Deployable Resources", © 1996 IEEE, Publ. No. 0-8186-7548-9/96, Pages 157-166.
JN	MORLEY, ROBERT E., Jr., et al., "A Massively Parallel Systolic Array Processor System", © 1988 IEEE, Publ. No. CH2603-9/88/0000/0217, Pages 217-225.
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JN	SCHMIT, HERMAN, "Incremental reconfiguration for pipelined applications," © 1997 IEEE, Publ. No. 0-8186-8159-4/97, Pages 47-55.
GN	SITKOFF, NATHAN, et al., "Implementing a Genetic Algorithm on a Parallel Custom Computing Machine", Publ. No. 0-8186-7086-X/95, Pages 180-187.
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GN	TANGEN, UWE, et al., "A parallel hardware evolvable computer POLYP extended abstract", © 1997 IEEE, Publ. No. 0-8186-8159/4/97, Pages 238-239.
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JN	"Information Brief", PCI Bus Technology, © IBM Personal Computer Company, 1997, Pages 1-3.

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